NanoXplore News on NG-Medium and NG-Ultra

NG medium

ESCC — European Space Components Coordination

QUALIFIED

We are proud to announce NanoXplore 65nm NG-MEDIUM FPGA ESCC QPL certification. This is an extremely important milestone for European space products. NG-MEDIUM is the first European FPGA to reach this maturity stage.
We expect to obtain similar qualifications for our upcoming new generation 28nm FDSOI technology product family in the near future.
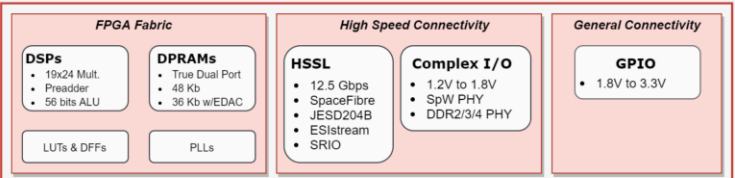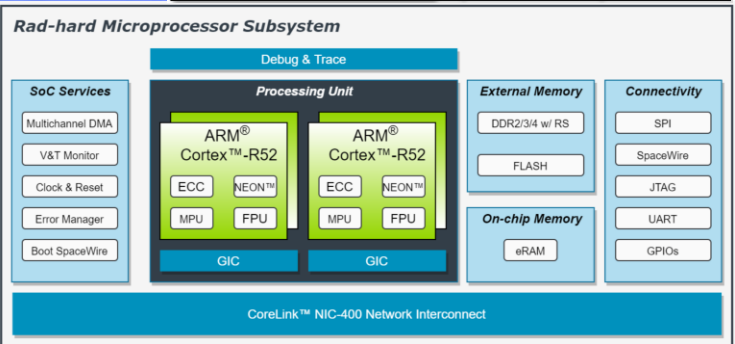
NG ultra

New released NX Impulse Design Suite

A proprietary design suite developed by NanoXplore to support its entire Radiation Hardened FPGA portfolio.

Impulse offers a complete compile design flow which transforms user HDL RTL code into a bitstream for dedicated NX devices through *Synthesise*, *Place* and *Route* software steps. It includes its own synthesis and static timing analysis tool.
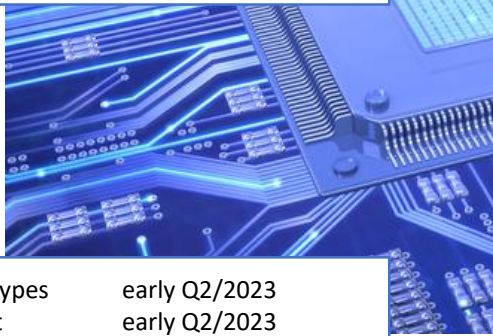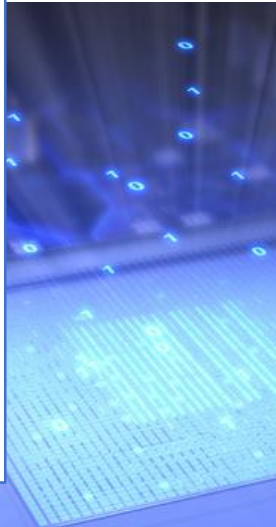
Device		Details	NX2H540TSC
Capacity			
ASIC Gates	Rad Hard FPGA		8 000 000
Logic Modules		16x Tiles + 8CGBs	
Register		384DFF on 16rows	505 344
LUT-4		408LUT on 16rows	536 928
Carry		96CY on 16rows	126 336
Embedded RAM			33Mb
DPRAM		672RAM * 48Kb	32.256K
Core Register File		672RF *2*2	2 688
Core Register File Bits		2688*32*18bits	1 512K Hardened
Clocks / PLL			50 / 7
Additional Features			
SpaceWire PHY (8 IOBs)	Rad Hard SOC	2x/Complex IOBank	20
DDR3/4 PHY (11IOBs)		2x/Complex IOBank	20
DSP Blocks		From 8 rows	1344
SpaceWire link I/F 430Mbps		CODEC	1
SERDES Tx/Rx 12,5Gbps		8 Quad x 4 SERDES	32
Hard IP Processor core		ARM Cortex-R52	4
SoC Peripherals		DALHIA	YES
Design Security			YES
Inputs / Outputs			-
Complex I/O bank	I/O	VIO 1,2 – 1,5 – 1,8V	10x 34 IOs
Simple I/O bank		VIO 1,8 – 2,5 – 3,3V	4x 24 IOs
Packages - User I/Os	PKG		740 I/Os
LF1752 & CF1752		45*45mm / 1mm	436 + SoC 304
FF1760		45*45mm / 1mm	436 + SoC 304

Rad-hard Microprocessor Subsystem

Debug & Trace

SoC Services	Processing Unit	External Memory	Connectivity
Multichannel DMA	ARM® Cortex™-R52 / ARM® Cortex™-R52 (ECC, NEON™, MPU, FPU)	DDR2/3/4 w/ RS	SPI
V&T Monitor		FLASH	SpaceWire
Clock & Reset			JTAG
Error Manager	GIC / GIC	On-chip Memory	UART
Boot SpaceWire		eRAM	GPIOs

CoreLink™ NIC-400 Network Interconnect

FPGA Fabric
- DSPs
  - 19x24 Mult.
  - Preadder
  - 56 bits ALU
- DPRAMs
  - True Dual Port
  - 48 Kb
  - 36 Kb w/EDAC
- LUTs & DFFs
- PLLs

High Speed Connectivity
- HSSL
  - 12.5 Gbps
  - SpaceFibre
  - JESD204B
  - ESIstream
  - SRIO
- Complex I/O
  - 1.2V to 1.8V
  - SpW PHY
  - DDR2/3/4 PHY

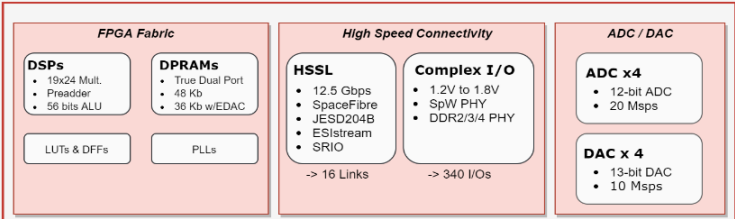**General Connectivity**
- GPIO
  - 1.8V to 3.3V

Rad-hard Programmable Logic

Prototypes   early Q2/2023
EvalKit   early Q2/2023

ESCC9000P equivalent FM Q4/2023

ESA Qual to be completed end of Q2/2024

NG ultra 300

Prototypes Q1/2024

FPGA Fabric
- DSPs
  - 19x24 Mult.
  - Preadder
  - 56 bits ALU
- DPRAMs
  - True Dual Port
  - 48 Kb
  - 36 Kb w/EDAC
- LUTs & DFFs
- PLLs

High Speed Connectivity
- HSSL
  - 12.5 Gbps
  - SpaceFibre
  - JESD204B
  - ESIstream
  - SRIO
- Complex I/O
  - 1.2V to 1.8V
  - SpW PHY
  - DDR2/3/4 PHY
- -> 16 Links
- -> 340 I/Os

ADC / DAC
- ADC x4
  - 12-bit ADC
  - 20 Msps
- DAC x 4
  - 13-bit DAC
  - 10 Msps

Rad-hard Programmable Logic